WHAT IS CLAIMED IS:

1. A processor, comprising:

an instruction set comprising a single-syllable IP-relative branch instruction and a long IP-relative branch instruction; the long IP-relative branch instruction occupying multiple syllables of an instruction bundle;

a first branch execution unit, the first branch execution unit comprising an adder to A) in a first mode, calculate a branch target of a single-syllable IP-relative branch instruction located in a first syllable of an instruction bundle, and B) in a second mode, calculate a branch target of a long IP-relative branch instruction located in said first syllable and a second syllable of an instruction bundle;

a second branch execution unit to calculate a branch target of a single-syllable IP-relative branch instruction located in said second syllable of an instruction bundle; and

wires, routed over the first branch execution unit, to provide bits in said second syllable of an instruction bundle to both the first and second branch execution units.

2. The processor of claim 1, wherein the first and second branch execution units are physically adjacent each other.

3. The processor of claim 1, wherein:

single-syllable IP-relative branch instructions carry M offset bits;

long IP-relative branch instructions carry N offset bits in said first syllable of an instruction bundle, and P offset bits in said second syllable of an instruction bundle; and

the wires alternately carry said M offset bits of single-syllable IP-relative branch instructions carried in said second syllable of an instruction bundle, or said P offset bits of a long IP-relative branch instruction.

4. The processor of claim 3, further comprising a multiplexer, the multiplexer comprising:

first data inputs coupled to receive a number of sign extension bits; and

second data inputs coupled to receive the P offset bits of a long IP-relative branch instruction;

wherein, when the first branch execution unit is configured in the first mode, the multiplexer outputs the number of sign extension bits which are received at its first data inputs, and said number of sign extension bits are merged with the M offset bits of a single-syllable IP-relative branch instruction to form at least part of said addend which is added to an instruction pointer value; and

wherein, when the first branch execution unit is configured in the second mode, the multiplexer outputs the P offset bits of a long IP-relative branch instruction which are received at its second data inputs, and said P offset bits are merged with the N offset bits of the same long IP-relative branch instruction to form at least part of said addend which is added to an instruction pointer value.

4. The processor of claim 3, wherein the wires are coupled to the second data inputs of the multiplexer.

5. The processor of claim 3, wherein a merger of the N and P offset bits of a long IP-relative branch instruction provide an offset which, when added to an instruction pointer value, is capable of redirecting an instruction pointer to an address of any instruction bundle stored in the processor's address space.

6. The processor of claim 3, wherein M=N.

7. The processor of claim 1, wherein each instruction bundle consists of three instruction syllables.

8. The processor of claim 7, wherein each instruction bundle further comprises a template field, wherein one state of the template field maps a first syllable of an instruction bundle to a memory execution unit, and maps second and third syllables of an instruction bundle to the first branch execution unit.

9. A processor, comprising:

an instruction set comprising a single-syllable IP-relative branch instruction and a long IP-relative branch instruction; the long IP-relative branch instruction occupying multiple syllables of an instruction bundle;

first and second branch execution units;

wires, routed over the first branch execution unit, to provide bits of a syllable of an instruction bundle to both the first and second branch execution units; and

a multiplexer comprising first data inputs coupled to receive a number of sign extension bits, and second data inputs coupled to receive from said wires offset bits of a long IP-relative branch instruction; the multiplexer outputting the number of sign extension bits to the first branch execution unit when the first branch execution unit is configured to calculate a branch target of a single IP-relative branch instruction, and the multiplexer outputting the offset bits of a long IP-relative branch instruction to the first branch execution unit when the first branch execution unit is configured to calculate a target for a long IP-relative branch instruction.

10. A method, comprising:

routing to first and second branch execution units, wires that carry bits of an instruction syllable of an instruction bundle; the wires being routed over the first branch execution unit; and

when the first branch execution unit is configured to calculate a branch target of a long IP-relative branch instruction occupying

multiple syllables of an instruction bundle, coupling the wires to the first branch execution unit, and otherwise not coupling the wires to the first branch execution unit.

11. The method of claim 10, further comprising:

when a branch target of a long IP-relative branch instruction is being calculated by the first branch execution unit, filling a first number of bit positions of an addend input of an adder of said first branch execution unit with bits carried over said wires, and filling a second number of bit positions of the addend input of said adder with additional offset bits supplied by a second instruction syllable of a long IP-relative branch instruction; and

when a branch target of a single-syllable IP-relative branch instruction is being calculated by the first branch execution unit, filling the first number of bit positions of the addend input of said adder with offset bits supplied by a single-syllable IP-relative branch instruction, and filling the second number of bit positions of the addend input of said adder with a number of sign extension bits.